	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
1			US 20050182587 A1	20050818	48	Circuit quality evaluation method and apparatus, circuit quality evaluation program, and medium having the program recorded thereon	702/117		702/117
2	X		US 20050182586 A1	20050818	6	Digital circuit for frequency and timing characterization	702/117		702/117
3	X		US 20050182585 A1	20050818	5	Structure and method for package burn-in testing	702/117		702/117
4	X		US 20050182584 A1	20050818	23	Method and system for identifying and locating defects in an integrated circuit	702/117		702/117
5	X		US 20050182583 A1	20050818		Testing apparatus	702/117		702/117
6	X		US 20050177334 A1	20050811		Resistance value calculation method	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
7	X		US 20050171718 A1	20050804		Apparatus for testing a device with a high frequency signal	702/117		702/117
8	X		US 20050171717 A1	20050804		Method and apparatus for creating variable delay	702/117		702/117
9	X		US 20050171716 A1	20050804		Attenuator test system	702/117		702/117
10	X		US 20050165572 A1	20050728		Systems and methods for non-intrusive testing of signals between circuits	702/117		702/117
11	X		US 20050149205 A1	20050707		Internal bias measure with onboard ADC for electronic devices	700/10	702/117	702/117
12	X		US 20050143946 A1	20050630		Method and apparatus for head write capability measurement in self test	702/117	360/39	702/117
13	X		US 20050143945 A1	20050630		Automatic exchange of degraders in accelerated testing of computer chips	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
14	X		US 20050125184 A1	20050609		Method and apparatus for monitoring integrated circuit fabrication	702/117	702/116; 702/127; 702/132; 702/184	702/117
15	X		US 20050119778 A1	20050602		CODING METHOD WITH DYNAMIC POSITIONING	700/121	702/117	702/117
16	X		US 20050114065 A1	20050526		Test system, test method and test program for an integrated circuit by IDDQ testing	702/117		702/117
17	X		US 20050114064 A1	20050526		Circuit for a parallel bit test of a semiconductor memory device and method thereof	702/117		702/117
18	X		US 20050114063 A1	20050526		Semiconductor device and testing circuit which can carries out a verifying test effectively for non-volatile memory cells	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
19	X		US 20050107975 A1	20050519		Method of diagnosing circuit layout and computer system for performing the same	702/117		702/117
20	X		US 20050107974 A1	20050519		Method for testing displays	702/113	702/117; 702/123; 702/126	702/117
21	X		US 20050096862 A1	20050505		AUTO-LINKING OF FUNCTION LOGIC STATE WITH TESTCASE REGRESSION LIST	702/117		702/117
22	X		US 20050090998 A1	20050428		Sensor signal processor	702/117		702/117
23	X		US 20050086019 A1	20050421		METHOD AND APPARATUS FOR TESTING A BRIDGE CIRCUIT	702/117		702/117
24	X		US 20050080582 A1	20050414		Method of adjusting strobe timing and function testing device for semiconductor device	702/117		702/117
25	X		US 20050080581 A1	20050414		Built-in self test for memory interconnect testing	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
26	X		US 20050080580 A1	20050414		Device for testing lsi to be measured, jitter analyzer, and phase difference detector	702/117		702/117
27	X		US 20050075820 A1	20050407		Method for checking test points of printed circuit board layout text data before plotting the printed circuit board layout map	702/117		702/117
28	X		US 20050075819 A1	20050407		ADAPTIVE LITHOGRAPHIC CRITICAL DIMENSION ENHANCEMENT	702/117		702/117
29	X		US 20050071108 A1	20050331		Method and apparatus for automated testing of display signals	702/117		702/117
30	X		US 20050060115 A1	20050317		Low profile carrier for non-wafer form device testing	702/108	702/117	702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
31	X		US 20050055172 A1	20050310		Photocontrol devices having flexible mounted photosensors and methods of calibrating the same	702/117		702/117
32	X		US 20050049812 A1	20050303		UNIVERSAL TEST PLATFORM AND TEST METHOD FOR LATCH-UP	702/117		702/117
33	X		US 20050049811 A1	20050303		System and method for indication of fuse defects based upon analysis of fuse test data	702/117		702/117
34	X		US 20050049810 A1	20050303		METHOD AND SYSTEM FOR DETERMINING MINIMUM POST PRODUCTION TEST TIME REQUIRED ON AN INTEGRATED CIRCUIT DEVICE TO ACHIEVE OPTIMUM RELIABILITY	702/117		702/117
35	X		US 20050043912 A1	20050224		Memory testing apparatus and method	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
36	X		US 20050038622 A1	20050217		Method and system for rerouteable cyclic redundancy check sum (CRC) for different sources	702/117		702/117
37	X		US 20050033541 A1	20050210		Memory cell signal window testing apparatus	702/117		702/117
38	X		US 20050033540 A1	20050210		Universal sensor adapter	702/117		702/117
39	X		US 20050027469 A1	20050203		De-embedding devices under test	702/117		702/117
40	X		US 20050015214 A1	20050120		Measuring constraint parameters at different combinations of circuit parameters	702/117		702/117
41	X		US 20050015213 A1	20050120		Method and apparatus for testing an electronic device	702/117		702/117
42	X		US 20040267481 A1	20041230		Apparatus and method for testing memory cards	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
43	X		US 20040267480 A1	20041230		Selective control of test-access ports in integrated circuits	702/117		702/117
44	X		US 20040267479 A1	20041230		Automatic self test of an integrated circuit component via AC I/O loopback	702/117		702/117
45	X		US 20040267478 A1	20041230		Methods and apparatus for analyzing flutter test data using damped sine curve fitting	702/117		702/117
46	X		US 20040260503 A1	20041223		Inspecting apparatus for semiconductor device	702/117		702/117
47	X		US 20040260502 A1	20041223		Accelerated test method and system	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
48	X		US 20040260501 A1	20041223		Method and circuit for detecting a fault of semiconductor circuit elements and use thereof in electronic regulators of braking force and of dynamics movement of vehicles	702/117		702/117
49	X		US 20040254756 A1	20041216		Internal bias measure with onboard ADC for electronic devices	702/117		702/117
50	X		US 20040254755 A1	20041216		Method and apparatus for automatically configuring and/or inserting chip resources for manufacturing tests	702/117		702/117
51	X		US 20040236530 A1	20041125		System and method of heating up a semiconductor device in a standard test environment	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
52	X		US 20040230396 A1	20041118		Method and apparatus for monitoring integrated circuit fabrication	702/117		702/117
53	X		US 20040230395 A1	20041118		Universally accessible fully programmable memory built-in self-test (MBIST) system and method	702/117		702/117
54	X		US 20040216537 A1	20041104		Continuous test flow method and apparatus	73/865.9	209/552; 324/765; 438/14; 702/117	702/117
55	X		US 20040210413 A1	20041021		Dynamic creation and modification of wafer test maps during wafer testing	702/117		702/117
56	X		US 20040204893 A1	20041014		Instruction register and access port gated clock for scan cells	702/117		702/117
57	X		US 20040204892 A1	20041014		Testing of integrated circuits from design documentation	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
58	X		US 20040204891 A1	20041014		Semiconductor memory device having a test mode for testing an operation state	702/117		702/117
59	X		US 20040186678 A1	20040923		SENSING CIRCUIT FOR SINGLE BIT-LINE SEMICONDUCTOR MEMORY DEVICE	702/117		702/117
60	X		US 20040183578 A1	20040923		Mixed signal delay locked loop characterization engine	327/161	702/117; 703/14	702/117
61	X		US 20040172211 A1	20040902		Test wafer usage forecast modeling method	702/117		702/117
62	X		US 20040167739 A1	20040826		Clock diagnostics	702/117		702/117
63	X		US 20040162693 A1	20040819		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117		702/117
64	X		US 20040162692 A1	20040819		Method and apparatus for monitoring integrated circuit fabrication	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
65	X		US 20040153279 A1	20040805		Method and apparatus for monitoring integrated circuit fabrication	702/117		702/117
66	X		US 20040153278 A1	20040805		Signal flow driven circuit physical synthesis technique	702/117		702/117
67	X		US 20040153277 A1	20040805		Analytical parasitic constraints generation technique	702/117		702/117
68	X		US 20040153276 A1	20040805		Method and apparatus for reduced pin count package connection verification	702/117		702/117
69	X		US 20040153275 A1	20040805		Novel test structure for detecting bridging of DRAM capacitors	702/117	257/E21.648	702/117
70	X		US 20040153274 A1	20040805		Fail analysis device	702/117		702/117
71	X		US 20040148121 A1	20040729		On-chip test mechanism for transceiver power amplifier and oscillator frequency	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
72	X		US 20040148120 A1	20040729		Method and apparatus for monitoring integrated circuit fabrication	702/117		702/117
73	X		US 20040148119 A1	20040729		Semiconductor test apparatus	702/117		702/117
74	X		US 20040143411 A1	20040722		Test handling apparatus and method	702/117	324/158.1 ; 324/765	702/117
75	X		US 20040111231 A1	20040610		INTEGRATED CIRCUITS HAVING POST-SILICON ADJUSTMENT CONTROL	702/117		702/117
76	X		US 20040102916 A1	20040527		Method for testing I/O ports of a computer motherboard	702/117		702/117
77	X		US 20040088131 A1	20040506		System and method for generating a shmoo plot by avoiding testing in failing regions	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
78	X		US 20040083073 A1	20040429		Probe testing method and apparatus for determining acceptable/defective end shape of contact probe through image analysis	702/117		702/117
79	X		US 20040083072 A1	20040429		Controlling the timing of test modes in a multiple processor system	702/117		702/117
80	X		US 20040054491 A1	20040318		Apparatus and method for testing socket	702/117		702/117
81	X		US 20040034495 A1	20040219		Method for determining fault coverage from RTL description	702/117		702/117
82	X		US 20040024556 A1	20040205		Method for testing chip configuration settings	702/117		702/117
83	X		US 20040024555 A1	20040205		Testing interface for railroad signal relays	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
84	X		US 20040019450 A1	20040129		Method for determining the critical path of an integrated circuit	702/117		702/117
85	X		US 20040019449 A1	20040129		In-system testing of an oscillator	702/117		702/117
86	X		US 20040015314 A1	20040122		System and method for the functional testing of semiconductor memory chips	702/117		702/117
87	X		US 20040015313 A1	20040122		Method for testing a device and a test configuration including a device with a test memory	702/117	257/E23.179; 702/14	702/117
88	X		US 20030233207 A1	20031218		Apparatus and method for testing a computer system by utilizing FPGA and programmable memory module	702/117		702/117
89	X		US 20030229466 A1	20031211		Test method and apparatus for source synchronous signals	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
90	X		US 20030220758 A1	20031127		Method for testing an AD-converter	702/117		702/117
91	X		US 20030212522 A1	20031113		Externally controllable electronic test program	702/117		702/117
92	X		US 20030204354 A1	20031030		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117		702/117
93	X		US 20030204353 A1	20031030		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117		702/117
94	X		US 20030204352 A1	20031030		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117		702/117
95	X		US 20030204351 A1	20031030		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
96	X		US 20030204350 A1	20031030		Method and apparatus for measuring the quality of delay test patterns	702/117		702/117
97	X		US 20030204349 A1	20031030		Data-based control of integrated circuits	702/117		702/117
98	X		US 20030200046 A1	20031023		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117		702/117
99	X		US 20030200045 A1	20031023		Input/output characterization chain for an integrated circuit	702/117		702/117
100	X		US 20030200044 A1	20031023		Systems and methods for tagging measurement values	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
101	X		US 20030195715 A1	20031016		Automatic test vector generation method, test method making use of the test vectors as automatically generated, chip manufacturing method and automatic test vector generation program	702/117		702/117
102	X		US 20030191601 A1	20031009		Method for overflow testing of a blind equalizer	702/117		702/117
103	X		US 20030171888 A1	20030911		Method for testing characteristics of oscillators	702/117		702/117
104	X		US 20030158688 A1	20030821		Method and apparatus for testing a system-on-a-chip	702/117		702/117
105	X		US 20030158687 A1	20030821		Composite eye diagrams	702/117		702/117
106	X		US 20030158616 A1	20030821		Program conversion system	700/97	702/117	702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
107	X		US 20030139892 A1	20030724		Method for connecting test bench elements and shell device	702/117		702/117
108	X		US 20030135345 A1	20030717		Process and circuit arrangement to monitor physical parameters	702/117		702/117
109	X		US 20030135344 A1	20030717		Methods for embedding and de-embedding balanced networks	702/117		702/117
110	X		US 20030135343 A1	20030717		Methods and apparatus for testing electronic devices	702/117		702/117
111	X		US 20030125895 A1	20030703		Apparatus and method for inspecting working operations on circuit substrate, and system and method for fabricating electric circuit	702/117		702/117
112	X		US 20030115008 A1	20030619		Test fixture with adjustable pitch for network measurement	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
113	X		US 20030088379 A1	20030508		Electron beam test system and electron beam test method	702/117		702/117
114	X		US 20030088378 A1	20030508		Method for determining poor performing cells	702/117		702/117
115	X		US 20030083840 A1	20030501		Apparatus and method for determining effect of on-chip noise on signal propagation	702/117		702/117
116	X		US 20030083839 A1	20030501		RF fixture electronics for testing RF devices	702/117		702/117
117	X		US 20030083838 A1	20030501		Wireless test and measurement method	702/117		702/117
118	X		US 20030083837 A1	20030501		Wireles test and measurement system	702/117		702/117
119	X		US 20030074152 A1	20030417		System and method of testing non-volatile memory cells	702/117		702/117
120	X		US 20030065470 A1	20030403		Method for in-service RAM testing	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
121	X		US 20030046015 A1	20030306		Test circuit and semiconductor integrated circuit effectively carrying out verification of connection of nodes	702/117		702/117
122	X		US 20030036869 A1	20030220		Using clock gating or signal gating to partition a device for fault isolation and diagnostic data collection	702/117		702/117
123	X		US 20030033107 A1	20030213		Method and apparatus for independent output driver calibration	702/117		702/117
124	X		US 20030028341 A1	20030206		Power on self test (POST) and extended self test (EST) for ultrasonic imaging system	702/117		702/117
125	X		US 20030004669 A1	20030102		System and method for testing time-varying signals	702/117		702/117
126	X		US 20020198674 A1	20021226		Method for testing integrated circuits	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
127	X		US 20020193960 A1	20021219		Method for operating a TAP controller and corresponding TAP controller	702/120	702/117	702/117
128	X		US 20020193959 A1	20021219		System and method of determining the noise sensitivity characterization for an unknown circuit	702/117		702/117
129	X		US 20020183955 A1	20021205		Test device for dynamic memory modules	702/117		702/117
130	X		US 20020183954 A1	20021205		Processing system for a wiring harness, a method for testing an electrical connection of a wiring harness, computer-readable storage medium and a wire connection assisting system	702/117		702/117
131	X		US 20020183953 A1	20021205		Method of fault isolation of a digital electronic device	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
132	X		US 20020183952 A1	20021205		Data path evaluation system and method	702/117		702/117
133	X		US 20020152046 A1	20021017		Concurrent control of semiconductor parametric testing	702/117		702/117
134	X		US 20020147559 A1	20021010		Method for testing integrated logic circuits	702/117		702/117
135	X		US 20020143486 A1	20021003		Method and apparatus for evaluating and correcting the tester derating factor (TDF) in a test environment	702/117		702/117
136	X		US 20020128794 A1	20020912		Semiconductor device having self test function	702/117		702/117
137	X		US 20020123854 A1	20020905		JTAG-based software to perform cumulative array repair	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
138	X		US 20020107650 A1	20020808		Methods and systems for determining a critical dimension and a presence of defects on a specimen	702/81	257/E21.53; 702/117	702/117
139	X		US 20020087285 A1	20020704		Universal serial bus test system	702/117		702/117
140	X		US 20020087284 A1	20020704		Method of protecting a circuit arrangement for processing data	702/117		702/117
141	X		US 20020087280 A1	20020704		Dynamic current calibrated driver circuit	702/107	702/117	702/117
142	X		US 20020082796 A1	20020627		Method for determining failure rate and selecting best burn-in time	702/120	702/117	702/117
143	X		US 20020082795 A1	20020627		Method and apparatus for error detection/correction	702/117		702/117
144	X		US 20020078400 A1	20020620		Self-test with split, asymmetric controlled driver output stage	714/30	702/117	702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
145	X		US 20020077763 A1	20020620		Automatic tester having separate coarse and precise timing modules	702/120	702/117	702/117
146	X		US 20020072872 A1	20020613		Method for diagnosing process parameter variations from measurements in analog circuits	702/117	257/E21.525	702/117
147	X		US 20020072871 A1	20020613		Circuit to indicate the status of a supply voltage	702/117	702/176	702/117
148	X		US 20020069027 A1	20020606		Arrangement and method of testing an integrated circuit	702/117		702/117
149	X		US 20020069026 A1	20020606		Semiconductor device capable of test mode operation	702/117		702/117
150	X		US 20020052705 A1	20020502		Testing method of semiconductor integrated circuit and equipment thereof	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
151	X		US 20020052704 A1	20020502		Communication interface unit, connection tool for test, wrap test tool, and wrap testing mehtod	702/117		702/117
152	X		US 20020038191 A1	20020328		Data head writer coil testing	702/117	702/108	702/117
153	X		US 20020032537 A1	20020314		Method and system for testing RAMBUS memory modules	702/117		702/117
154	X		US 20020029124 A1	20020307		Method for testing a CMOS integrated circuit	702/117		702/117
155	X		US 20020029123 A1	20020307		Semiconductor device and semiconductor device testing method	702/117		702/117
156	X		US 20020016693 A1	20020207		Method for fabricating and checking structures of electronic circuits in a semiconductor substrate	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
157	X		US 20020010560 A1	20020124		System for mapping logical functional test data of logical integrated circuits to physical representation using pruned diagnostic list	702/118	702/117	702/117
158	X		US 20020010559 A1	20020124		Semiconductor device having a mode of functional test	702/117		702/117
159	X		US 20020007253 A1	20020117		Noise analyzing method and apparatus and storage medium	702/111	702/117	702/117
160	X		US 20010053960 A1	20011220		Adjustment method for reducing channel skew of test system	702/85	702/117	702/117
161	X		US 20010041967 A1	20011115		Semiconductor device testing apparatus and method for testing semiconductor device	702/117		702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
162	X		US 20010029436 A1	20011011		Semiconductor electrical characteristics evaluation apparatus and semiconductor electrical characteristics evaluation method	702/117		702/117
163	X		US 20010023392 A1	20010920		Abnormality detection device for detecting an abnormality in a communication bus	702/120	702/117	702/117
164	X		US 20010007970 A1	20010712		Automatic test vector generation method, test method making use of the test vectors as automatically generated, chip manufacturing method and automatic test vector generation program	702/117	702/120	702/117
165	X		US 20010005817 A1	20010628		Circuit trace probe and method	702/117	702/108	702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
166	X		US 20010002461 A1	20010531		Circuit and method for specifying performance parameters in integrated circuits	702/120	702/117	702/117

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
1			US 20050171719 A1	20050804	37	System and method for measuring essential power amplification functions	702/120		702/120
2	X		US 20050154552 A1	20050714	27	Methods for delay-fault testing in field-programmable gate arrays	702/120		702/120
3			US 20050096863 A1	20050505	9	System and method for testing a component in a computer system using voltage margining	702/120		702/120
4	X		US 20050075821 A1	20050407	7	Method for testing circuit units to be tested and test apparatus	702/120		702/120
5	X		US 20050071109 A1	20050331	16	Media platform testing	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
6	X		US 20050065747 A1	20050324	16	Mixed-signal core design for concurrent testing of mixed-signal, analog, and digital components	702/120		702/120
7	X		US 20050060116 A1	20050317	16	Method and apparatus for performing testing of interconnections	702/120		702/120
8	X		US 20050049813 A1	20050303	9	Method for facilitating a test person to identify a test program item in server test	702/120		702/120
9	X		US 20050033543 A1	20050210	13	System and method for testing of transaction initiation devices in electronic funds transfer systems	702/120		702/120
10	X		US 20050027471 A1	20050203	15	Method and apparatus for smoothing current consumption in an integrated circuit	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
11	X		US 20050027470 A1	20050203	27	Interactive stub apparatus for testing a program and stub program storage medium	702/120		702/120
12	X		US 20040267487 A1	20041230	13	Apparatus and method for testing non-deterministic device data	702/120		702/120
13	X		US 20040267486 A1	20041230	30	Use of I2C-based potentiometers to enable voltage rail variation under BMC control	702/120		702/120
14	X		US 20040243337 A1	20041202	24	Adapting scan architectures for low power operation	702/120		702/120
15	X		US 20040243336 A1	20041202	19	Examination request management apparatus	702/120		702/120
16	X		US 20040236533 A1	20041125	22	Test substrate reclamation method and apparatus	702/120		702/120
17	X		US 20040236532 A1	20041125	16	Integrated circuit with parameter measurement	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
18	X		US 20040225466 A1	20041111	16	Testing apparatus, method of controlling the same, and program for implementing the method	702/120		702/120
19	X		US 20040148123 A1	20040729	12	Semiconductor device having a test circuit for testing an output circuit	702/120		702/120
20	X		US 20040148122 A1	20040729	13	Method for testing signal paths between an integrated circuit wafer and a wafer tester	702/120		702/120
21	X		US 20040102917 A1	20040527	32	Apparatus for testing I/O ports of a computer motherboard	702/120		702/120
22	X		US 20040064285 A1	20040401	21	Automated circuit board test actuator system	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
23	X		US 20040059537 A1	20040325	6	TEST MODE CONTROL CIRCUIT FOR RECONFIGURING A DEVICE PIN OF AN INTEGRATED CIRCUIT CHIP	702/120		702/120
24	X		US 20040059536 A1	20040325	21	Multiple sweep point testing of circuit devices	702/120		702/120
25	X		US 20040054492 A1	20040318	10	Methods and systems for enhanced automated system testing	702/120		702/120
26	X		US 20040002832 A1	20040101	11	Method and apparatus for boundary scan of serial interfaces	702/120		702/120
27	X		US 20030220760 A1	20031127	11	Universal diagnostic platform for specimen analysis	702/120		702/120
28	X		US 20030220759 A1	20031127		Fail analyzer	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
29	X		US 20030212524 A1	20031113		Test access circuit and method of accessing embedded test controllers in integrated circuit modules	702/120		702/120
30	X		US 20030200049 A1	20031023		Electronic test program with run selection	702/120		702/120
31	X		US 20030167145 A1	20030904		Test apparatus	702/120		702/120
32	X		US 20030163273 A1	20030828		Hybrid tester architecture	702/120		702/120
33	X		US 20030158691 A1	20030821		Systems and methods for facilitating testing of pad receivers of integrated circuits	702/120		702/120
34	X		US 20030158690 A1	20030821		Systems and methods for facilitating automated test equipment functionality within integrated circuits	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
35	X		US 20030158689 A1	20030821		Method for extracting parasitic capacitances of field-effect transistors	702/120		702/120
36	X		US 20030109995 A1	20030612		Method of deducing equivalent circuit and system for the same	702/64	702/120	702/120
37	X		US 20030101015 A1	20030529		Method and apparatus for testing, characterizing and tuning a chip interface	702/120		702/120
38	X		US 20030083841 A1	20030501		Method and apparatus for enabling extests to be performed in AC-coupled systems	702/120		702/120
39	X		US 20030078752 A1	20030424		SYSTEM AND METHOD FOR TESTING A CIRCUIT IMPLEMENTED ON A PROGRAMMABLE LOGIC DEVICE	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
40	X		US 20030055592 A1	20030320		System and method for analyzing error information from a semiconductor fabrication process	702/120	257/E21.525	702/120
41	X		US 20030028342 A1	20030206		Method for the defect analysis of memory modules	702/120		702/120
42	X		US 20030014208 A1	20030116		Apparatus and method for testing computer equipment for use in networks	702/120		702/120
43	X		US 20020193960 A1	20021219		Method for operating a TAP controller and corresponding TAP controller	702/120	702/117	702/120
44	X		US 20020183956 A1	20021205		Testing compliance of a device with a bus protocol	702/120		702/120
45	X		US 20020173926 A1	20021121		Method and system for wafer and device-level testing of an integrated circuit	702/120		702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
46	X		US 20020138227 A1	20020926		Data computation apparatus and method for using the data computation apparatus for adjustment of electronic controller	702/120		702/120
47	X		US 20020116142 A1	20020822		Signal inspection device	702/120		702/120
48	X		US 20020107654 A1	20020808		Apparatus for testing semiconductor integrated circuit	702/120		702/120
49	X		US 20020103611 A1	20020801		System and method for receiving information from a test apparatus	702/120		702/120
50	X		US 20020082796 A1	20020627		Method for determining failure rate and selecting best burn-in time	702/120	702/117	702/120
51	X		US 20020077763 A1	20020620		Automatic tester having separate coarse and precise timing modules	702/120	702/117	702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
52	X		US 20020062200 A1	20020523		Tester for semiconductor integrated circuits and method for testing semiconductor integrated circuits	702/120		702/120
53	X		US 20020059040 A1	20020516		Network diagnostic meter	702/120		702/120
54	X		US 20020035442 A1	20020321		Hierarchical test circuit structure for chips with multiple circuit blocks	702/120		702/120
55	X		US 20010025227 A1	20010927		Monitored burn-in test system and monitored burn-in test method of microcomputers	702/120		702/120
56	X		US 20010023392 A1	20010920		Abnormality detection device for detecting an abnormality in a communication bus	702/120	702/117	702/120

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif
57	X		US 20010007970 A1	20010712		Automatic test vector generation method, test method making use of the test vectors as automatically generated, chip manufacturing method and automatic test vector generation program	702/117	702/120	702/120
58	X		US 20010002461 A1	20010531		Circuit and method for specifying performance parameters in integrated circuits	702/120	702/117	702/120

	Type	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	41	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:56	
2	BRS	10	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:56	
3	BRS	6	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output) with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:56	
4	BRS	1	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output) and terminal$1 with shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:50	
5	BRS	6	test$3 with first with (IC$1 or integrated adj circuit$1) with chip$1 and (i/o or input/output) and terminal$1 with shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:50	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
6	BRS	105	(ICs or integrated adj circuits) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
7	BRS	101	multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
8	BRS	3	multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
9	BRS	0	test$3 with multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
10	BRS	7	test$3 with (IC$1 or integrated adj circuit$1) with combin$6 with package with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
11	BRS	35	test$3 with (IC$1 or integrated adj circuit$1) with shar$3 with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:06	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
12	BRS	3	test$3 with first with (IC$1 or integrated adj circuit$1) with shar$3 with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:07	
13	BRS	19	test$3 with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with semiconductor$1 and (isolat$3 or tri-stat$3 or disconnect$3) with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with connect$4 with (power$3 or electric$4) and terminal$1 and memory and (power$3 or electric$4) with (down or shutdown or disconnect$3) and (test$3 or operat$3) with mode$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:07	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
14	BRS	9	test$3 with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with semiconductor$1 and (isolat$3 or tri-stat$3 or disconnect$3) with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with connect$4 with (power$3 or electric$4) and terminal$1 and memory and (power$3 or electric$4) with (down or shutdown or disconnect$3) and (test$3 or operat$3) with mode$1 and shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:49	
15	BRS	47	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:50	
16	BRS	12	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:51	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
17	BRS	7	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output) with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:02	
18	BRS	2	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output) and terminal$1 with shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:13	
19	BRS	7	test$3 with first with (IC$1 or integrated adj circuit$1) with chip$1 and (i/o or input/output) and terminal$1 with shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:18	
20	BRS	109	(ICs or integrated adj circuits) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:18	
21	BRS	105	multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:19	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
22	IS&R	2	("4531068").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:42	
23	IS&R	2	("6351681").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:55	
24	BRS	51	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:56	
25	BRS	13	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:56	
26	BRS	8	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output) with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:56	
27	BRS	117	(ICs or integrated adj circuits) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
28	BRS	112	multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
29	BRS	3	multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
30	BRS	0	test$3 with multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
31	BRS	7	test$3 with (IC$1 or integrated adj circuit$1) with combin$6 with package with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 11:57	
32	BRS	38	test$3 with (IC$1 or integrated adj circuit$1) with shar$3 with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:06	
33	BRS	4	test$3 with first with (IC$1 or integrated adj circuit$1) with shar$3 with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:07	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
34	BRS	20	test$3 with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with semiconductor$1 and (isolat$3 or tri-stat$3 or disconnect$3) with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with connect$4 with (power$3 or electric$4) and terminal$1 and memory and (power$3 or electric$4) with (down or shutdown or disconnect$3) and (test$3 or operat$3) with mode$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:08	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
35	BRS	9	test$3 with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with semiconductor$1 and (isolat$3 or tri-stat$3 or disconnect$3) with (IC$1 or integrated adj circuit$1 or wafer$1 or chip$1 or die$1) with connect$4 with (power$3 or electric$4) and terminal$1 and memory and (power$3 or electric$4) with (down or shutdown or disconnect$3) and (test$3 or operat$3) with mode$1 and shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:49	
36	BRS	8	test$3 with first with (IC$1 or integrated adj circuit$1) with chip$1 and (i/o or input/output) and terminal$1 with shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:50	
37	BRS	51	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:50	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
38	BRS	13	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 12:51	
39	BRS	8	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output) with terminal$1	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:02	
40	BRS	2	set$4 with up with (IC$1 or integrated adj circuit$1) with chip$1 with test$3 and (i/o or input/output) and terminal$1 with shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:14	
41	BRS	8	test$3 with first with (IC$1 or integrated adj circuit$1) with chip$1 and (i/o or input/output) and terminal$1 with shar$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:18	
42	BRS	117	(ICs or integrated adj circuits) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2005/08/30 13:18	

	Type	Hits	Search Text	DBs	Time Stamp	Comments
43	BRS	112	multiple with (IC$1 or integrated adj circuit$1) with combin$6 with package	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM TDB	2005/08/30 13:19	